

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 2 as follows:

This application is a divisional application of U.S. Patent Application Serial No. 10/163,925, filed June 6, 2002, which claims the benefit of U.S. Provisional Application Serial No. 60/340,001 filed December 10, 2001, the disclosures ~~disclosure~~ of which are is incorporated herein by reference in their entireties ~~its entirety~~.

Please replace the paragraph beginning at page 4, line 8 with the following:

With reference to FIG. 1, a plurality of isolation regions 10 formed in a layer of semiconductor material 12 is illustrated. The isolation regions 10 define the size and placement of active regions 14, from which semiconductor devices 16 can be constructed. In the illustrated embodiment, the semiconductor devices 16 are MOSFETs. Thus, the semiconductor devices 16 will sometimes be referred to herein as MOSFETs 18. The illustrated MOSFETs 18 include an NMOS device 18n and a PMOS device 18p, ~~81p~~. Accordingly, FIG. 1 illustrates a portion of a wafer 19 having a plurality of semiconductor devices 16 and isolation regions 10 formed thereon.

Please replace the paragraph beginning at page 6, line 22 with the following:

The MOSFETs 18 are formed using respective active regions 14 disposed between adjacent sets of isolation regions 10. Each MOSFET 18 includes a source 28, a drain 30 and a body 32 disposed between the source 28 and the drain 30. In the illustrated embodiment, the source 28 ~~20~~ and the drain 30 ~~22~~ each include a deep doped region and an extension region as illustrated. Each MOSFET 18 also includes a gate 34. The gate 34 is disposed on the layer of semiconductor material 12 over the body 32 and defines a channel within the body 32 (the channel being interposed between the source 28 and the drain 30).